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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,453	09/16/2003	Mitsuhiro Sugimoto	4633-0107P	2514

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EXAMINER	
CALEY, MICHAEL H	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,453	SUGIMOTO ET AL.	
	Examiner	Art Unit	
	Michael H. Caley	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7 and 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/29/05 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2-7 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U.S. Patent No. 6,639,589 "Kim").

Regarding claims 1, 12, and 13, Kim discloses a display device having:

a display panel (Figure 4 element 202) and a plurality of wiring boards (Figure 4 elements 210, 210'; Column 3 lines 23-25) placed along a periphery of the display panel,

wherein the display panel has panel side connection wiring (Figure 4 element 248) for electrically connecting a first wiring board (Figure 4 element 211') and a second

wiring board (Figure 4 element 211) adjacent to each other among the plurality of wiring boards,

each of the plurality of wiring boards having an insulating base (Figure 4 elements 211 and 211'), a board-side wiring group (Figure 4 elements 213, 214, 215, 213', 214', and 215'), and at least one driving circuit element for driving the display panel (Figure 4 elements 212 and 212'),

the board-side wiring group is composed of element-connected wiring (Figure 4 element 213 and 213'; Column 5 lines 25-30) electrically connected to the driving circuit element, first non-connected wiring (Figure 4 element 214, 214') having no electrical connection to the driving circuit element (Column 8 lines 54-60) and second non-connected wiring (Figure 4 element 214, 214) having no electrical connection to the driving circuit element (element 214 is necessarily composed of multiple lines; Column 6 lines 44-49), and

the panel-side connection wiring is formed so that the element connected wiring of the first wiring board (Figure 4 element 213'; Column 5 lines 25-30) and the first non-connected wiring of the second wiring board (Figure 4 element 214; Column 5 lines 9-10) are electrically connected to each other (Column 6 line 47) and so that the first non-connecting wiring of the first wiring board (Figure 4 element 214'; Column 5 lines 9-10) is connected to the second non-connecting wiring of the second wiring board (Figure 4 element 214; Column 6 line 48);

wherein the plurality of wiring boards as having wiring patterns identical in board-side wiring group (Figure 4 elements 210 and 210').

Regarding claim 3, Kim discloses

a plurality of lines constituting the board-side wiring group as running on the insulating base without crossing each other (Figure 4 element 210),

the non-connected wiring (Figure 4 element 214) as in a roughly U shape as viewed from top with both ends at the periphery of the insulating base, and

at least one end of the element-connected wiring is located inside or outside both ends of the non-connected wiring at the periphery of the insulating base, or the element-connected wiring is interposed between a plurality of lines of the non-connected wiring.

Regarding claim 4, Kim discloses the non-connected wiring as having another roughly U shape as viewed from top in at least a portion near one end extending in a direction away from the other end (Figure 4 element 214).

Regarding claim 5, Kim discloses each of the plurality of wiring board (Figure 5 element 210 in portions "I" and "II") as having n or n+1 sets of lines (Figure 5 elements 281, 282, and 283) that constitute the board-side wiring group and are involved in signal transmission where n is the total number of driving circuit elements (2) of the plurality of wiring boards.

Regarding claim 6, Kim discloses each wiring board as further having board-side spare wiring electrically connected to the driving circuit element (Figure 4 element 215),

the display panel further having gate lines (Figure 4 element 241), source lines (Figure 4 element 242) crossing the gate lines, switching element electrically connected to the gate lines and the source lines (Column 4 lines 1-14), pixel electrodes connected to the gate lines and the source lines via the switching elements (Column 4 lines 11-14), and panel-side spare wiring electrically connected to the board side spare wiring (Figure 4 element 245), and

the panel-side spare wiring (element 245) crosses the source lines (element 242) via an insulating film near both ends of the source lines.

It is noted that the insulating film between the intersection of lines 245 and 242 is not explicitly mentioned by Kim. Such an insulation film, however, is an inherent feature between source lines and the spare wiring "gate lines" assembled and intersecting on a common substrate, such as disclosed by Kim. Such an insulation film is necessary to separate the lines at the intersection points and is also known as a gate insulation film or layer.

Regarding claim 7, Kim discloses the display panel as a liquid crystal panel (abstract).

Regarding claim 14, Kim discloses a display device having:

a display panel (Figure 4 element 202) having panel side connection wiring (Figure 4 elements 247 and 248);

a first wiring board (Figure 4 element 210) having an insulating base (Figure 4 element 211), a driving circuit element (Figure 4 element 212), a first wiring path (Figure 4 element 213, Figure 5 element 283) connected to the driving circuit element, a second

wiring path and a third wiring path (Figure 4 element 213, Figure 5 elements 282 and 281); and

a second wiring board identical to the first wiring board (Figure 4 element 210');

wherein the panel-side connection wiring connects the second wiring path of the first wiring board to the first wiring path of the second wiring board (Figure 5 element 282).

Regarding claim 15, Kim discloses the panel-side wiring as connecting the third wiring path of the first board to the second wiring path of the second board (Figure 5 element 281).

Response to Arguments

Applicant's arguments filed 8/29/05 and raised during the interview on 1/4/06 have been fully considered but they are not persuasive.

At the outset, it is noted that Figure 5 of Kim and the descriptions thereof are no longer relied upon for the rejection of claims 2 and 14, although the examiner maintains that the subject matter described in connection to Figure 5 is intended by Kim to be coexisting in a same embodiment with the subject matter of Figure 4. It is also noted that wiring board 210' is designated as the first wiring board and 210 is designated as the second wiring board, which is a change from the rejection presented in the previous office action.

Applicant contends that Figure 4 fails to disclose the proposed wiring connections between the first and second wiring boards. The examiner disagrees and maintains the rejection as presented above. Elements 213 and 213' refer only to element-connected wirings (Column 5

lines 8-9, lines 21-24). Elements 214 and 214' refer only to non-connected wiring having no electrical connection to the driving circuit element (Column 5 lines 9-10, lines 35-41). Column 6 lines 44-49 disclose that a first group of the non-connecting wiring on the second board (214) is connected to the element connected wiring of the first board (213') and a second group of the non-connecting wiring on the second board (214) is connected to a first group of the non-connecting wiring on the first board (214').

Due to the above interpretation of Figure 4 aided by the reference's Detailed Description, the Examiner is convinced that there is no contradiction between the wiring patterns shown and described in Figures 4 and 5. Figure 5 appears to show a schematic description of three specific gate driving signal line groups and is clearly not intended to show every wiring pattern in connection with the wiring boards as many have been obviously omitted. Furthermore the statement "As described referring to FIGS. 2 to 6..." (Column 8 line 45) explicitly indicates that Figures 4 and 5 included in the group coexist in a mutual embodiment. Elements 281, 282, and 283 are used as examples of the wiring groups 213 and 214 (Column 8 lines 45-53).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael H. Caley whose telephone number is (571) 272-2286. The examiner can normally be reached on M-F 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael H. Caley
January 7, 2005
mhc

ANDREW SCHECHTER
PRIMARY EXAMINER